ĐẠI HỌC QUỐC GIA TP. HỒ CHÍ MINH
TRƯỜNG ĐẠI HỌC CÔNG NGHỆ THÔNG TIN

SUBJECT SYLLABUS
< CE222 – DIGITAL INTEGRATED CIRCUIT DESIGN>

1. GENERAL INFORMATION

Course name (English):	Digital Integrated Circuit Design
Course code:	CE222
Level:	General course ☐; Basic IT course ☐; Junior CE core course ☐; Senior CE core course ☑; Graduating course ☐
Faculty/Department:	Computer Engineering/Integrated Circuits and Hardware Design
Instructor:	Dr. Lâm Đức Khải
Credits:	4
Lecture:	3
Laboratory:	1
Self-Study:	6
Pre-requisite:	Introduction to Digital Circuits, Digital Logic Design

2. COURSE DESCRIPTIONS

The course introduces to students:

- Fundamental knowledge of digital integrated circuits design.
- Methodologies to analyze, design, simulation and layout the basic digital circuits at CMOS level.
- Design schematics, do simulation, do layout and verify the integrated circuits of combinational circuits and sequential circuits.

3. COURSE GOALS

After taking the course, students are able to:

- Understand the fundamental knowledge of digital integrated circuits design.
- Be able to analyze, design, simulation and layout the basic and advanced digital circuits at CMOS level, such as combinational circuits and sequential circuits.
- Be able to use EDA tools to analyze, design, simulation and layout the digital integrated circuits.

Table 1.

Index	Course Goals*[1]*	Program Outcomes[2]
G1	Be able to analyze digital integrated circuits	3.1
G2	Be able to be "long-life" learning	5.2
G3	Develop the professional ethics	6.1
G4	Be able to read the English reference material	9.2
G5	Be able to design digital integrated circuits	10.2

4. COURSE LEARNING OUTCOMES - LO

Table 2.

Learning outcomes (LO)	Course learning outcome descriptions [2]	Program Outcomes[2]
G1 (3.1.2)	Be able to analyze function, performance of digital integrated circuits	T
G2 (5.2)	Be able to self-study by search, read and understand related material.	I, U
G3 (6.1.2)	Be able to develop the professional ethics	T
G4 (9.2.2)	Be able to read and explain English reference books	U
G5 (10.2.2)	Be able to design digital integrated circuits	T, U

5. COURSE CONTENT AND LECTURE PLAN

a. LECTURES

Table 3.

Lecture (3 lecture-hours) *[1]*	Contents *[2]*	LO *[3]*	Teaching and Learning Activities *[4]*	Assessment schemes *[5]*
Lecture 1, 2	**Chương 1: Introduction** 1.1 Semiconductor	G2, G4	**Instructor:** - Introduce about the course	

	evolution 1.2 Integrated Circuit (IC) 1.3 Problems in IC design		syllabus - Introduce about fundamental of digital integrated circuits and their applications - Discussion with students about problems needed to b deal with during IC design. **Student:** - Try to understand the goals of this course - Note the main points of lecture 1 and 2. - Thinking, asking, answering and discussing with instructor. - Solve the problems and homeworks of chapter 1	A1, A2
Lecture 3, 4	**Chapter 2: CMOS Logic and Layout** 2.1 A Brief History 2.2 CMOS Gate Design 2.3 Pass Transistors 2.4 CMOS Latchs and Flip-Flops 2.5 Standard Cells Layouts 2.6 Stick Diagrams	G2, G4	**Instructor:** - Check the problems and homeworks of chapter 1 that are solved by students, then review knowledge of chapter 1 by asking several questions to students. - Present how to design circuits and layouts the basic logic gates using CMOS technologies. - Present how to stick diagram of layout - Raise several questions about draw schematics and layout, stick diagram of several logic gates for students to discuss **Students:** - Read lecture note and reference books of chapter 2 before class. - Note the main points of lecture 3, 4 - Thinking, asking, answering and discussing with instructor. - Solve the problems and homeworks of chapter 2	A1, A2
Lecture 5, 6	**Chương 3: Ideal MOS Transistor Theory**	G2, G4	**Instructor:** - Check the problems and	

	3.1 Introduction 3.2 MOS Capacitance 3.3 nMOS I-V Characteristics 3.4 pMOS Characteristics 3.5 Gate and Diffusion Capacitances		homeworks of chapter 2 that are solved by students, then review knowledge of chapter 2 by asking several questions to students. - Explain the operations of nMOS and pMOS in the ideal conditions - Show how to derive the I-V characteristics of nMOS and pMOS. - Present the effects of Gate and Diffusion capacitances on I-V characteristics. - Raise several questions about relations between I-V characteristics for students to discuss **Students:** - Read lecture note and reference books of chapter 3 before class. - Note the main points of lecture 5, 6 - Thinking, asking, answering and discussing with instructor. - Solve the problems and homeworks of chapter 3	A1, A2
Lecture 7, 8	**Chapter 4: Non-Ideal MOS Transistor Theory** 4.1 Introduction 4.2 Electric Field Effect 4.3 Channel Length Modulation 4.4 Threshold Voltage Effects 4.5 Leakage	G2, G4	**Instructor:** - Check the problems and homeworks of chapter 3 that are solved by students, then review knowledge of chapter 3 by asking several questions to students. - Explain the operations of nMOS and pMOS in the non-ideal conditions. - Show the effects of electric field, channel length modulation, threshold voltage and leakage to the I-V characteristics of nMOS and pMOS. - Raise several questions about effects of electric field, channel length	A1, A4

			modulation, threshold voltage and leakage on MOS for students to discuss **Students:** - Read lecture note and reference books of chapter 4 before class. - Note the main points of lecture 7, 8 - Thinking, asking, answering and discussing with instructor. - Solve the problems and homeworks of chapter 4	
Lecture 9, 10	**Chapter 5: DC and Transient Response** 5.1 Pass Transistor 5.2 DC Response 5.3 Noise Margin 5.4 Transient Response 5.5 RC Delay Model 5.6 Delay Estimation	G1, G5	**Instructor:** - Check the problems and homeworks of chapter 4 that are solved by students, then review knowledge of chapter 4 by asking several questions to students. - Explain the purpose of DC and Transient analysises in IC design. - Present the meaning of Noise Margin and how to calculate it - Present how to estimate the delay in IC circuit using RC model - Raise several examples on how to estimate delay of several circuits for students to discuss **Students:** - Read lecture note and reference books of chapter 5 before class. - Note the main points of lecture 9, 10 - Thinking, asking, answering and discussing with instructor. - Solve the problems and homeworks of chapter 5	A1, A4
Lecture 11, 12	**Chương 6: Logical Effort** 6.1 RC Delay Estimation 6.2 Logical Effort 6.3 Delay in a Logic Gate	G1, G5	**Instructor:** - Check the problems and homeworks of chapter 5 that are solved by students,	A1, A4

	6.4 Delay in Multistage Logic Networks 6.5 Choosing the Best Number of Stages 6.6 Example		then review knowledge of chapter 5 by asking several questions to students. - Present another method to estimate delay in IC design using logical effort . - Show on how to choose the best number of stages and the gate sizes of each stages for minimum delay. - Raise several examples on how to estimate delay in IC design using logical effort and choose the best number of stages and the gate sizes of each stages for students to discuss. **Students:** - Read lecture note and reference books of chapter 6 before class. - Note the main points of lecture 11, 12 - Thinking, asking, answering and discussing with instructor. - Solve the problems and homeworks of chapter 6	
Lecture 13, 14	**Chapter 7: Power** 7.1 Introduction 7.2 Power Consumption 7.3 Dynamic Power 7.4 Static Power	G1, G5	**Instructor:** - Check the problems and homeworks of chapter 6 that are solved by students, then review knowledge of chapter 6 by asking several questions to students. - Present about the sources of power consumption in IC circuits. - Show the methods to minimize the power consumption in IC design - Raise several questions about power consumption and how to minimize it in IC design for students to discuss. **Students:** - Read lecture note and reference books of chapter	A1, A4

			7 before class. - Note the main points of lecture 13, 14 - Thinking, asking, answering and discussing with instructor. - Solve the problems and homeworks of chapter 7	
Lecture 15	**Chương 8: Circuit Simulation SPICE** 8.1 Introduction 8.2 DC Analysis in SPICE 8.3 Transient Analysis in SPICE 8.4 Spice Netlist 8.5 Current, Voltage, Delay and Power Measurements	G1, G5	**Instructor:** - Check the problems and homeworks of chapter 7 that are solved by students, then review knowledge of chapter 7 by asking several questions to students. - Instruct how to use SPICE to simulate, measure the functions, timing delay and power consumption of IC designs in DC or Transient analysises. - Raise several questions about use SPICE to simulate, measure the functions, timing delay and power consumption of IC designs for students to discuss **Students:** - Read lecture note and reference books of chapter 8 before class. - Note the main points of lecture 15 - Thinking, asking, answering and discussing with instructor. - Solve the problems and homeworks of chapter 8	A1, A4

b. LABORATORY

Table 4.

Lab (5 lab-hours)	**Contents** *[2]*	**LO** *[3]*	**Teaching and Learning Activities** *[4]*	**Assessment schemes** *[5]*
Lab 1	**Lab 1:** Using Synopsys-Custom	G1, G3, G5	**Instructor:** - Instruct how to read the lab guide	A3

	Design to design IC circuits		- Instruct how to use Synopsys-Custom Design to design IC circuits. - Answer any questions from students **Students:** - Follow a step by step on the lab guide to design circuit, simulation and layout for simple IC circuit using Synopsys-Custom Design tool - Verify the results on waveform of SPICE simulation - Do the draft report about what students done. - Finish the report of Lab 1 at home	
Lab 2	**Lab 2:** IC Design, Simulation, Layout for the combinational circuit: Adder	G1, G3, G5	**Instructor:** - Instruct how to design, simplify the Adder circuit using CMOS technology. - Answer any questions from students **Students:** - Derive the Adder logic expressions, then design circuit, pre-layout simulation and layout, extract RC, post-layout simulation for Adder circuit. - Verify the results on waveform of SPICE simulation - Do the draft report about what students done. - Finish the report of Lab 2 at home	A3
Lab 3	**Lab 3:** IC Design, Simulation, Layout for the sequential circuit: D-flipflop	G1, G3, G5	**Instructor:** - Instruct how to design, simplify the D-flipflop circuit using CMOS technology. - Answer any questions from students **Students:**	A3

			- Derive the D-flipflop logic expressions, then design circuit, pre-layout simulation and layout, extract RC, post-layout simulation for D-flipflop circuit. - Verify the results on waveform of SPICE simulation - Do the draft report about what students done. - Finish the report of Lab 3 at home	
Lab 4	**Lab 4:** IC Design, Simulation, Layout for the complex circuit: ALU-4bit	G1, G3, G5	**Instructor:** - Instruct how to design, simplify the ALU-4bit circuit using CMOS technology. - Answer any questions from students **Students:** - Derive the ALU-4bit logic expressions, then design circuit, pre-layout simulation and layout, extract RC, post-layout simulation for ALU-4bit circuit. - Verify the results on waveform of SPICE simulation - Do the draft report about what students done. - Finish the report of Lab 4 at home	A3
Lab 5	**Lab 5:** IC Design, Simulation, Layout for the compex circuit: Datapath of simple processor	G1, G3, G5	**Instructor:** - Instruct how to design, simplify the datapath of simple processor circuit using CMOS technology. - Answer any questions from students **Students:** - Derive the datapath of simple processor logic expressions, then design circuit, pre-layout simulation and layout,	A3

			extract RC, post-layout simulation for datapath of simple processorcircuit. - Verify the results on waveform of SPICE simulation - Do the draft report about what students done. - Finish the report of Lab 5 at home	
Lab 6	**Lab 6:** IC Design, Simulation, Layout for the compex circuit: Simple processor	G1, G3, G5	**Instructor:** - Instruct how to design a controller of simple processor circuit using CMOS technology. - Instruct how to connect the datapath and controller circuits to build a simple processor. - Answer any questions from students **Students:** - Derive the controller of simple processor logic expressions, then design circuit, pre-layout simulation and layout, extract RC, post-layout simulation for datapath of simple processor circuit. - Connect the datapath and controller circuits and layout to build a simple processor - Verify the results on waveform of SPICE simulation. - Do the draft report about what students done. - Finish the report of Lab 6 at home**.**	A3

6. COURSE ASSESSMENT

Table 5. Assessment schemes

Assessment schemes *[1]*	**LO** *[2]*	**Percentage (%)** *[3]*
A1. Attendance,	*G2, G3*	*15%*

Quizes, Homeworks		
A2. Mid-term exam	*G2, G4*	*15%*
A3. Laboratory	*G1, G3, G5*	*20%*
A4. Final-term exam	*G1, G5*	*50%*

Table 6: **Rubric assessment for A1-A4 schemes**

Assessment schemes	Chapter	Points			
		0-3	4-5	6-8	9-10
A1, A2, A3	Chapter 1	Understand structure and operations of PN junction	Understand structure and operations of NMOS/ PMOS gates	Understand the fabrication procedure for NMOS/ PMOS	Be able to design schematic and layout for basic gates
A1, A2, A3	Chapter 2	Be able to design schematic and layout for simple logic expressions at CMOS level	Be able to design schematic and layout for specific logic gates at CMOS level, such as transmission gate, tristate, mux	Be able to design schematic and layout, stick diagram for sequential logic gates at CMOS level, such as D-latch, D-Flipflop	Understand clearly about race conditions in IC designs Be able to estimate the area of layout design
A1, A2	Chapter 3	Understand on how to form the operation modes of MOS capacitors	Be able to explain 3 operation modes of NMOS/ PMOS	Be able to derive the I-V expressions of 3 operation modes for NMOS/PMOS.	Understand the capacitances formed during operations of NMOS/PMOS
A1, A4	Chapter 4	Understand the effects of electric field on operations of NMOS/ PMOS	Understand the effects of channel length modulation on operations of NMOS/ PMOS	Understand the effects of threshold voltage on operations of NMOS/ PMOS	Understand the effects of leakage current on operations of NMOS/ PMOS Understand the effects of technology and environment on operations of NMOS/ PMOS
A1, A4, A3	Chapter 5	Be able to explain about DC and Transient analysis and	Be able to do DC and Transient analysis for basic CMOS	Be able to explain the phenomenons cause the propagration	Be able to model the CMOS circuits using Elmore delay model

		their purposes in IC design	gates Understand the meaning of Noise Margin	delays in IC design by using mathematic equations Be able to model the CMOS gates using Elmore delay model.	Be able to improve layout to minimize propagation delay causes by RC.
A1, A4	Chapter 6	Understand the meaning of effort delay, logical delay, electrical effort and parasitic delay	Be able to calculate the effort delay, logical delay, electrical effort and parasitic delay of basic CMOS gates	Understand the meaning of path logical effort, path electrical effort, path effort and branching effort Be able to calculate the path logical effort, path electrical effort, path effort and branching effort of the CMOS circuits	Be able to optimize the number of stages and the device sizes of gates in CMOS circuits to minizie the propagation delay.
A1, A4	Chapter 7	Understand the meaning of power consumption, dynamic and static power consumptions in IC design	Understand the sources of dynamic and static power consumptions in IC design	Be able to calculate the dynamic and static power consumptions in IC design	Be able to reduce the dynamic and static power consumptions in IC design
A1, A4, A3	Chapter 8	Understand the reasons of need SPICE for simulation and verification of IC design	Be able to use SPICE to do DC and Transient analysises for CMOS circuits design	Be able to optimize the CMOS gates in IC design by using SPICE	Be able to find the logical effort for CMOS gates in IC design by using SPICE

7. COURSE REQUIREMENTS

- Lecture class:

+ Attendance: not allow to absent more than 3 lectures, not allow to be late more than 15 minutes.

+ Always take the lecture note, book and notebook

+ Read lecture notes, do the homeworks before classes

- Laboratory:

+ Attendance: not allow to absent more than 2 labs, not allow to be late more than 15 minutes.

+ Follow the Lab guide to prepare the Lab content before each Lab class

8. BOOK AND REFERENCE BOOKS

Book:

1. Thiết kế vi mạch số, Nguyễn Minh Sơn, Nguyễn Trần Sơn, Đại học quốc gia Tp.HCM, Trường đại học Công nghệ thông tin, 1st Edition, 2016.

Reference books:

1. *CMOS VLSI Design,* Neil H.E .Weste, D. Harris, Pearson Education, Inc. Publishing as Pearson Addison-Wesley, 4th Edition, 2011.

2. *Digital Integrated Circuit - A Design Perspective*, J.Rabaey, A.Chandrakasan B.Nikolic, 2th Edition, 2002.

9. LAB TOOLS

1. T-**SPICE** for Simulation
2. **CADENCE/SYNOPSYS Student Edition** for Design

Date: August-05, 2018

Dean/Head of Department **Instructor**

Nguyễn Minh Sơn Lâm Đức Khải