VIETNAM NATIONAL UNIVERSITY – HO CHI MINH CITY

UNIVERSITY OF INFORMATION TECHNOLOGY

SYLLABUS
CE213 – DIGITAL SYSTEM DESIGN WITH HDL

1. GENERAL INFORMATION (Thông tin chung)

Course name (Vietnamese):	Thiết kế hệ thống số với HDL
Course name (English):	Digital System Design with HDL
Code:	CE213
Type of course:	General course ☐; Basic IT course ☐; Junior CE core course ☐; Senior CE core course ☑; Graduating course ☐
Deparment:	Faculty of Computer Engineering
Instructor:	M.Eng. Ho Ngoc Diem
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Number of credits:	4
Theory:	45
Lab:	30
Self-study:	90
Prerequisite course(s):	
Pre-course(s):	Introduction to Digital Circuits, Digital Logic Design

2. COURSE DESCRIPTION (Mô tả môn học)

This course aims to introducing the overview concepts of logic circuit design and fron-end IC design methods using hardware description language VHDL & Verilog.

3. COURSE GOALS (Mục tiêu môn học)

After completing this course, students can:

- Describe the steps of a digital IC design process and the role of hardware description language (HDL) in the digital design process. Know the design process based on ASIC and FPGA technology.

- Know Verilog hardware description language (mainly) and VHDL.

- Ability to design and use hardware description language to implement Digital designs at different descriptive levels.

- Ability to test the design by software through Testbench written in hardware description language.

Table 1.

Goal No.	Goal description *[1]*	Program outcomes *[2]*
G1	Analyze, reason and solve problems of designing a digital system using HDL language	*3.1, 3.2*
G2	Have skills to learn and research to solve scientific problems	*4.1*
G3	Skill in analyzing, synthesizing and thinking digital systems	*5.1*
G4	Raising awareness of responsibility for work, complying with practices in labs	*6.1*
G5	Know and use specialized English for the subject.	*9.2*

4. COURSE LEARNING OUTCOMES (Chuẩn đầu ra môn học)

Table 2.

Course outcomes *[1]*	Descriptions *[2]*	Level of teaching *[3]*

*G1.1 (*3.1.2*)*	**Analyze** the functions and tasks of blocks in a given design	T,U
*G1.2 (*3.2.2*)*	**Plan** and **design** the block diagram of the design from the statement of the problem. **Describe, build** and **operate** the system to check the design on software and hardware using HDL language	T,U
G2 (4.1.1)	**Know** and **apply** different design flows of HDL language to solve scientific problems	I,T
G3 (5.1.1, 5.2.2)	Knowledge of digital systems for analyzing and synthesizing the most optimal problem.	I,T
G4 (6.1.1, 6.1.2)	Have a sense of responsibility for the work assigned and the issues of compliance with Lab internal rules. Have positive attitudes in learning.	I,T,U
G5 (9.2.1, 9.2.2)	**Understand** and use specialized English terms of the subject. Have ability to read professional documents in foreign languages.	I,T

5. COURSE CONTENT, LESSON PLAN (Nội dung môn học, kế hoạch giảng dạy)

1. Theory

Table 3.

Week (3 lecture-hours) *[1]*	**Contents** *[2]*	**Course learning outcomes** *[3]*	**Activities** *[4]*	**Assessment element** *[5]*

Week (3 lecture-hours) *[1]*	Contents *[2]*	Course learning outcomes *[3]*	Activities *[4]*	Assessment element *[5]*
Week 1	**Chapter 0: Introducing the subject** 1. Introduce the course plan and course outline 2. Introduce the classroom 3. Introduce how to assess the subject **Chapter 1: Introduction** 1.1. Introducing Hardware description language Verilog, VHDL, and some related concepts 1.2. Process of digital IC design 1.3. Design support tools	*G3, G5*	**Preparation activities:** **Teacher:** Using the course website tool to inform the necessary information prepared for the subject including: subject lectures, lecturer information, and some notes before class - Inform students about the subject regulations **Student:** Download subject lectures, prepare subject and teacher's requirements on the subject website **Teaching activities:** **-** Lecture, present for students the content according to the lecture slides - Introduce students to practical examples: Common tools used in digital IC design - Introduce students to methods, practical tools, support for the subject **Learning activities:** Listening to lectures, talking with lecturers about related issues. **Home activities:** **-** Review the lesson learned - Learn, download tools, software for the subject: quartus 2, modelsim, synopsys	A1, A4
Week 2	**Chapter 2: Verilog - Basic concepts** 2.1. Semantic conventions	*G3, G5*	**Teaching activities:** - Lecture the content in the slide of the lesson - Use practical examples to	A1,A4

Week (3 lecture-hours) *[1]*	Contents *[2]*	Course learning outcomes *[3]*	Activities *[4]*	Assessment element *[5]*
	2.2. Datatypes 2.3. Connection rules 2.4. Introducing the design model (structure, behavior)		interpret students - Evaluate points for students with active activities - Teachers introduce the course projects to students. **Learning activities:** Listen to lectures and exchange knowledge related to the lesson **Home activities:** Students discuss to form groups and choose the project topic.	
Week 3	Chapter 3: Modules and hierarchical structure 3.1 Hierarchical structure 3.2 Module 3.3 Instance	*G3, G5*	**Teaching activities:** - Lecture for students the contents of the lesson - Introduce to students practical examples of verilog language. - Introduce a number of conventions commonly used in microchip companies - Give students a short test (10-15 minutes): use verilog language to apply the knowledge of creating basic digital circuit modules learned from previous subjects such as: circuit, subtraction, translation circuit . **Learning activities:** Listen to lectures and exchange relevant knowledge. Do some example exercises in the slide, and do the test given by the instructor. **Home activities:** - Students do homework No. 1	A1,A4

Week (3 lecture-hours) *[1]*	Contents *[2]*	Course learning outcomes *[3]*	Activities *[4]*	Assessment element *[5]*
			- Review the old lesson and prepare for the next lesson	
Week 4	**Chương 4: Primitive Gates – Switches – User defined primitives** 4.1. Primitive gates 4.2 Switches 4.3. User-defined primitives	G1.1, G5	**Teaching activities:** - Explain the contents of the lesson - Introduce to students practical examples of verilog language. - Introduce a number of conventions commonly used in microchip companies **Learning activities:** Listen to lectures and exchange relevant knowledge. Do some example exercises in the slides. **Test activities:** - Require students to do exercises in class to get process points: using the knowledge in section 4.1, 4.2, 4.3 describe common circuits: decoding, coding, mux .. - Use integrated tools to synthesize and compare results between methods (in case students have personal computers) **Home activities**: - Teacher: Creating exercise activities on Moodle. - Students: use the results in the exercises, write the simulation program and test on modelsim software, get the waveform analysis and submit the lesson to the moodle system.	A1,A4
Week 5, 6	**Chapter 5: Structure model** 5.1 Basic elements / gates 5.2 Transmission delay (Propagation	G1.2, G2, G5	**Teaching activities:** - Lecture for students the content of the lesson - Check the progress of implementing the course	A1,A4

Week (3 lecture-hours) *[1]*	Contents *[2]*	Course learning outcomes *[3]*	Activities *[4]*	Assessment element *[5]*
	delay): Inertial delay, Transport delay 5.3 User-defined basic elements - UDP (or Truth table model for combinational and sequential circuits with Verilog) 5.4. Some design illustrations		project of students. **Learning activities:** - Listen to lectures and exchange relevant knowledge. Do some example exercises in the slides. - Report of project implementation progress: presenting the achieved results and difficulties in the implementation process **Test activities:** Teacher: Require students to do test # 2, evaluate process points. SV: take a test and submit a paper copy **Home activities:** - Describe common digital circuits by different models. - Use synthesis tools to synthesize, analyze results and compare differences.	
Week 7	**Review**		**Teaching activities:** - Review the knowledge learned in half of the semester. - Give students some exercises in previous chapters. **Learning activities:** -Listen to lectures and exchange relevant knowledge. Doing exercises in class **Q&A:** Teachers spend 15-20 minutes at the end of the session for the questions and	A1

Week (3 lecture-hours) *[1]*	Contents *[2]*	Course learning outcomes *[3]*	Activities *[4]*	Assessment element *[5]*
			answers: check the learning status of students, assessing the ability of students to understand lessons in half semester. Answer questions and related issues from students. **Home activities:** - Teachers provide some homeworks for revision to prepare students for the midterm exams - Students review the midterm exam	
Week 8, 9, 10	**Chapter 6: Behavior model** 6.1. Behavior model based on Boolean algebra 6.2. Continuous assignment 6.3. Expressions in Verilog 6.4. Level-sensitive circuits and Latch in Verilog 6.5. Cycle behavior model - "always" block 6.6. Procedure assignment 6.7. Behavior model of some common circuits 6.8. Related design issues	G1.2, G2, G5	**Teaching activities:** - Introducing the behavioral model, comparing the advantages and disadvantages of the behavioral model to the structural model learned in the previous lessons. - Provide practical examples to help students understand better. **Students:** listening to lectures, exchanging relevant opinions. **Test activities:** Teacher: Let the students take the test No. 3 to evaluate the process score. Content of the test: using behavioral model to implement common digital circuits: addition, subtraction, comparison, decoding, coding .. **Home activities:** - Teacher: create online test number 2 for students on the course website. Content: Using behavioral model to perform circuits designed in test number 1. -	A1,A4

Week (3 lecture-hours) *[1]*	Contents *[2]*	Course learning outcomes *[3]*	Activities *[4]*	Assessment element *[5]*
			Students need to present the full design, analysis of simulation results, synthesis on the software - Students implement design, write simulation programs, and synthesize. Write a report of the results, and submit it to the course website on time	
Week 11	**Chapter 7: State machine** 7.1 Design Moore-style state machine 7.1 Design Mealy-type state machine	G1.2, G2, G5	**Teaching activities:** - Check the progress of students' course project implementation. Evaluate the results, and propose students to take the next steps to complete the best results. - Introduce students to state machine knowledge and use HDL language to describe a state machine **Learning activities:** - Report the progress of project implementation - Listen to lectures and talk with teachers about related knowledge **Home activities:** Teacher: Let students use verilog language to design a state machine. Use tools to simulate, and analyze synthesis results Students: Do homework, submit design results with hard copies	A1,A4
Buổi 12	**Chương 8: Functions and Tasks** 8.1 Function 8.2 Task 8.3 Generate structure	G1.2, G2	**Teaching activities:** - Lecture the contents of the lesson - Analyze and give practical examples about the difference and similarity between functions and tasks. - Use the generate structure **Learning activities:**	A1,A4

Week (3 lecture-hours) *[1]*	Contents *[2]*	Course learning outcomes *[3]*	Activities *[4]*	Assessment element *[5]*
			Listening to lectures, exchanging relevant opinions. **Home activities:** - Students review the lesson, prepare a lesson for chapter 9.	
Week 13	**Chapter 9: Simulation / Functional Verification** 9.1 Introducing test plan 9.2 Testbench 9.3. Techniques to create testcase 9.4 Simulation of the circuit 9.5 Introducing Coverage 9.4 Test method	G1.2, G2	**Teaching activities:** - Introduce students simulation process, circuit test, and introduce practical examples. - Guide students to use testing and simulation tools. - Share practical experience in the simulation process and checking digital circuits -Remind students to complete the course project. Introduce some rules and regulations in the project report process. -Guide students to present, and write reports for course projects. **Learning activities:** - Listen to lectures and exchange relevant knowledge. - Use personal computers to follow teachers' instructions. **Home activities:** Students complete the course projects.	A1,A4
Week 14	**Report course projects**	G1.1, G1.2, G2, , G3, G5	- Students report the results of the course project implementation - Teachers and students discuss questions related to the content of the subject	A1

Week (3 lecture-hours) *[1]*	Contents *[2]*	Course learning outcomes *[3]*	Activities *[4]*	Assessment element *[5]*
			- Teacher summarize the results of the project implementation, give the pros and cons of the students to promote their strengths and learn from the shortcomings.	
Week 15	**Ôn tập**	G1.1, G3	**Teaching activities:** - Teachers review the learned knowledge, note important knowledge - Give students to do some sample exercises, explain, analyze, and guide how to do it **Learning activities:** Students do exercises in class, exchange issues and questions.	A1

2. Lab (Thực hành)

Table 4.

Week (X hours) *[1]*	Contents *[2]*	Course learning outcomes *[3]*	Activities *[4]*	Assessment element *[5]*

Week (X hours) *[1]*	Contents *[2]*	Course learning outcomes *[3]*	Activities *[4]*	Assessment element *[5]*
Lab 1	**Instructions for practicing IC design using verilog on modelsim**	*G1.2, G2, G4*	**Teach:** Instructors explain to students the meaning of the exercise, guide students how to perform lab. **Study in class:** Students practice and verify the results at the class **Study at home:** Students read exercise and prepare in advance.	A3
Lab 2	Practice 2: Sequential circuit design by finite state machine model	*G1.2, G2, G4*	**Teach:** Instructors explain to students the meaning of the exercise, guide students how to perform lab. **Study in class:** Students practice and verify the results at the class **Study at home:** Students read exercise and prepare in advance.	A3
Lab 3	**ALU Design**	*G1.2, G2, G4*	**Teach:** Instructors explain to students the meaning of the exercise, guide students how to perform lab. **Study in class:** Students practice and verify the results at the class **Study at home:** Students read exercise and prepare in advance.	A3
Lab 4	**Design simple datapath**	*G1.2, G2, G4*	**Teach:** Instructors explain to students the meaning of the exercise, guide students how to perform lab. **Study in class:** Students practice and verify the results at the class **Study at home:** Students read exercise and prepare in advance.	A3
Lab 5	**Design Control unit**	*G1.2, G2, G4*	**Teach:** Instructors explain to students the meaning of the exercise, guide students how to perform lab. **Study in class:** Students practice and verify the results at the class **Study at home:** Students read exercise and prepare in advance.	A3
Lab 6	**Design simple processor**	*G1.2, G2, G4*	**Teach:** Instructors explain to students the meaning of the exercise, guide students how to	A3

Week (X hours) *[1]*	Contents *[2]*	Course learning outcomes *[3]*	Activities *[4]*	Assessment element *[5]*
			perform lab. **Study in class:** Students practice and verify the results at the class **Study at home:** Students read exercise and prepare in advance.	

6. COURSE ASSESSMENT (Đánh giá môn học)

Table 5.

Assessment element *[1]*	Course learning outcomes (Gx) *[2]*	Percentage (%) *[3]*
A1. Others (In-class test, attendance, presentation …)	*G4, G5*	*20%*
A2. Mid-term exam		*0%*
A3. Lab	*G1.2, G2, G4*	*30%*
A4. Final exam	*G1.1, G1.2, G2, G3, G5*	*50%*

1. **Rubric assessment for A1**

	8-10	**6-8**	**4-6**	**0-3**	**0**
Tests at class (5%)	Complete all tests in class.	Complete 75% of classroom tests.	Complete 50% of classroom tests.	Complete under 50% of classroom tests.	Don't take the test.
Homework(5%)	Complete all homeworks	Complete 75% homeworks	Complete 50% homeworks	Complete under 50% homeworks	Don't do homeworks.
Course projects (10%) The content of the project depends on each topic given by the lecturer during the semester.' Students will select the topic in the 3rd week of the semester, the duration of 10 weeks	Good report completion: - Full progress report - Presenting the content of the report fully and properly - Complete protection of the course project and answering the questions well.	Report completion: - Full progress report -Presentation of content has some minor errors. - Completing the protection of the project, not answering the questions well	Report completion: - There are reports of progress - A sketchy report - Not well protection of the report.	Incomplete the report: - Have progress reports - The report has not been completed. - Do not protect the project.	Don't perform the project.

2. **Rubric assessment for A2**

3. **Rubric assessment for A3**

	8-10	***6-8***	***4-6***	***0-3***	***0***
Lab 1 (5%)	Design and complete simulation of the sequential circuit	Complete design of the sequential circuit. Not complete the simulation of the design.	Pepare the lesson at home. .	Don't prepare the lesson at home.	No attendance
Lab 2 (5%)	Design and complete simulation of the sequential circuit under state machine model.	Complete design of the sequential circuit under state machine model. Not complete the simulation of the design	Pepare the lesson at home.	Don't prepare the lesson at home.	No attendance
Bài thực hành số 3 (5%)	Design and complete simulation of the ALU 4 bit.	Complete design of the ALU 4 bit. Not complete the simulation of the design.	Pepare the lesson at home.	Don't prepare the lesson at home.	No attendance
Lab 4 (5%)	Design and complete simulation of the dataparh for a simple MIPS processor.	Complete design of the datapath for a simple MIPS processor. Not complete the simulation of the design.	Pepare the lesson at home.	Don't prepare the lesson at home.	No attendance
Lab 5 (5%)	Design and complete simulation of	Complete design of the simple Control unit	Pepare the lesson at home.	Don't prepare the lesson at	No attendance

	the simple Control unit for a simple MIPS processor.	for a simple MIPS processor. Not complete the simulation of the design.		home.	
Lab 6 (5%)	Design and complete simulation of a simple processor using Verilog.	Complete design of a simple processor using Verilog. Not complete the simulation of the design.	Pepare the lesson at home.	Don't prepare the lesson at home.	No attendance

4. Rubric assessment for A4

General knowledge about HDL	***8-10***	***6-8***	***4-6***	***0-3***	***0***
Process of digital system design	List and fully explain the process of designing digital circuit system.	List advantages and disadvantages between the traditional methods of designing a digital system and today's method. Explain common terms used in the digital system design process	Correctly explain less than 50% of the common terms.	List but not fully explain the process of designing digital circuit system numbers.	Cannot describe process of designing digital circuit system.
General knowledge about HDL	Using the Primitive gates, UDP to design common combinational and sequential circuits: mux, decoder, adder, sub, encoder, counter	Using the Primitive gates, UDP to design common combinational and sequential circuits: mux, decoder, adder, sub, encoder, counter	Compare the difference between HDL hardware description language and programming language. Understand the basic concepts of verilog hardware description language. Not design or design incorrectly common combinational and sequential circuits.	List at least 3 popular HDL languages Cannot compare between the HDL hardware description language and the programming language. Don't understand the basic concepts of verilog language	Can only list 1-2 basic hardware description languages

Knowledge about structural model	Understand and apply effectively structural model in designing combinational and sequential circuits. Design popular digital circuits such as mux, decoder, adder, sub, encoder, counter and some other basic circuits using structural model	Understand and apply effectively structural model in designing combinational and sequential circuits. Design popular digital circuits such as mux, decoder, adder, sub, encoder, counter and some other basic circuits using structural model. However, there are still small errors in design process.	Understand and apply structural model in designing combinational and sequential circuits. Design 40-50% popular digital circuits such as mux, decoder, adder, sub, encoder, counter and some other basic circuits using structural model.	Understand but cannot apply structural model in designing combinational and sequential circuits.	Cannot understand structural model in designing combinational and sequential circuits.
Knowledge about behavioral model	Understand and apply effectively behavioral model in digital system design.	Understand and apply effectively behavioral model in digital system design.	Understand and apply behavioral model in digital system design.	Understand behavioral model in digital system design.	Don't understand behavioral model in digital system design.
	Design popular digital circuits such as mux, decoder, adder, sub, encoder, counter and some other basic circuits using behavioral model	Design popular digital circuits such as mux, decoder, adder, sub, encoder, counter and some other basic circuits using behavioral model.However, there are still small errors in design process.	Design 40-50% popular digital circuits such as mux, decoder, adder, sub, encoder, counter and some other basic circuits using behavioral model.	Cannot design popular digital circuit using behavioral model.	

Use state machine to design digital circuits.	Use Verilog to describe correctly Moore/Mealy State Machine.	Use Verilog to describe correctly 80% Moore/Mealy State Machine.	Use Verilog to describe correctly 50% Moore/Mealy State Machine.	Understand concept and differentiate between Moore and Mealy state machine. Cannot design Moore/Mealy State Machine using Verilog.	Don't understand concept of state machine.

7. COURSE REQUIREMENTS AND EXPECTATIONS (Quy định của môn học)

Class attendance: according to the general rule of the school

- Lab:

o Students attend full practice sessions according to instructors (GVHD). Students must prepare sections 1 through 3 in the "Practical Instructions" file before going to class. Instructors will check the preparation of the students in the first 15 minutes of the class (if there is no preparation, student is assumed to be absent in that lab).

o Students must run their design on ModelSim simulation software to check the design, then the instructor will check to complete the exercise.

o Details of the rules will be described in the practical guide

- Course project: students register as a group for a certain topic under the instructor's instructions.

- Actively do small exercises in class, and complete homework assignments

- Students read the slides of the course and the materials required by the instructor before each lesson.

8. COURSE MATERIALS (Tài liệu học tập, tham khảo)

Textbook:

1. Micheal D. Ciletti, ***Advanced Digital*** Design ***with the Verilog HDL***, 2nd Edition, Prentice Hall, 2010.

Reference books:

1. Vũ Đức Lung, Lâm Đức Khải, Phan Đình Duy, Giáo Trình Ngôn Ngữ Mô Tả Phần Cứng Verilog, Đại Học Công Nghệ Thông Tin, Đại học Quốc Gia Thành Phố Hồ Chí Minh.
2. IEEE Std 1364-2005 (Revision of IEEE Std 1364-2001), *IEEE Standard for Verilog Hardware Description Language*
3. D. R. Smith, P. D. Franzon, Verilog styles for synthesis, Prentice Hall 2000
4. Zainalabedin Navabi (2006). *Verilog Digital System Design*. McGraw-Hill
5. Samir Palnitkar (2003). *Verilog HDL 2nd Edition*. Prentice Hall,
6. Volnei A. Pedroni (2004). *Circuit Design with VHDL*. The MIT Press

9. SOFTWARE, TOOLS (Phần mềm, công cụ hỗ trợ thực hành)

1. Altera (Web Edition version). *Quartus II* (Version 13.0)
2. Terasic. *DE2 board*

HCMC, Jan 15th 2019

Faculty Head **Instructor**

(Ký và ghi rõ họ tên) *(Ký và ghi rõ họ tên)*