VIETNAM NATIONAL UNIVERSITY – HO CHI MINH CITY
UNIVERSITY OF INFORMATION TECHNOLOGY

SYLLABUS
CE118 – DIGITAL LOGIC DESIGN

1. GENERAL INFORMATION (Thông tin chung)

Course name (Vietnamese):	Thiết kế luận lý số
Course name (English):	Digital Logic Design
Code:	CE118
Type of course:	General course ☐; Basic IT course ☐; Junior CE core course ☑; Senior CE core course ☐; Graduating course ☐
Deparment:	Faculty of Computer Engineering
Instructor:	M.Eng. Ho Ngoc Diem
Number of credits:	4
Theory:	45
Lab:	30
Self-study:	90
Prerequisite course(s):	
Pre-course(s):	Introduction to Digital Circuits

2. COURSE DESCRIPTION (Mô tả môn học)

This course aims to provide students with a general view of the design method of digital circuits, from the basic level to the circuits that serve specific applications, and the process of designing a simple processor. The course provides the definitions and structures of registers, memories, finite-state-machines, datapath, control unit, latency, cost, and instruction sets. This course also provides students with the ability to analyze, design, evaluate, and synthesize digital systems.

3. COURSE GOALS (Mục tiêu môn học)

Table 1.

Goal No.	Goal description *[1]*	Program outcomes *[2]*
G1	**Ability to analyze and solve problems related to finite state machine, data path, control unit, processor design.**	*3.1, 3.2*
G2	**Ability to know and use different techniques in the processes of designing digital circuits.**	*4.1*
G3	**Ability of Lifelong learning**	*5.2*
G4	**Comprehensive reading skills**	*9.2*

4. COURSE LEARNING OUTCOMES (Chuẩn đầu ra môn học)

Table 2.

Course outcomes *[1]*	Descriptions *[2]*	Level of teaching *[3]*
G1.1 (3.1.2)	Ability to analyze finite state machine circuits, data paths, and control units.	*ITU*
G1.2 (3.2.2)	Ability to synthesize and optimize state machine circuits, datapaths, control units, and processor designs.	*ITU*
G2 (4.1.1)	Ability to know and use different techniques to optimize the circuits, analyze the cost and latency of the circuits, use ASM and FSMD models in the design process.	ITU
G3 (5.2)	Ability to self-study, self-research and comprehend relevant academic materials	*IU*
G3	Ability to comprehend professional materials	*IU*

5. COURSE CONTENT, LESSON PLAN (Nội dung môn học, kế hoạch giảng dạy)

a. Theory

Table 3.

Week (3 lectur e-	Contents *[2]*	Course learning outcomes *[3]*	Activities *[4]*	Assessment element *[5]*

hours) *[1]*				
Week 1	**Chapter 1: Sequential Logic** 1.1. SR Latch 1.2. Gated SR Latcha. 1.3. Gated D Latch 1.4. Other Flip-Flops .	*G1.1, G1.2, G3, G4*	**Teaching:** -Examining students'knowledge about basic digital circuit (studied in the previous course: Introduction to Digital Circuits) - Review basic sequential components **Learning:** - Asking, answering and discussing. - Reading reference textbook 1: 6.1-6.5 from pages 213 to 229. - Do related exercises in the main reference book. Read the content of the next session.	*A1, A2*
Week 2	**Chapter 1: Sequential Logic (cont.)** 1.5. Analysis of Sequential Logic 1.6. Finite State Machine Model	*G1.1, G1.2, G2, G3, G4*	**Teaching:** - Check previous lecture and homework. -Explain and give examples of analyzing a sequential ciruit. - Describe components of a finite state machine. **Learning:** - Asking, answering and discussing. - Reading reference textbook 1: 6.6-6.8 from pages 230 to 242. - Do related exercises in the main reference book. Read the content of the next session.	A1, A2
Week 3	**Chapter 1: Sequential Logic (cont.)** 1.7. Synthesis of Sequential Logic 1.7.1. State Minimization 1.7.2. State Encoding	*G1.1, G1.2, G2, G3, G4*	**Teaching:** -Explain method and give examples of how to minize states, encode states, and choose fliplops in term of circuit cost and latency optimization. **Learning:** - Asking, answering and discussing. - Reading reference textbook 1: 6.9-6.11 from pages 242 to 257. - Do related exercises in the main reference book. Read the content of the next session.	*A1, A2*
Week 4	**Chapter 1: Sequential Logic (cont.)** 1.8. Choice of memory elements 1.9. Optimization and	*G1.1, G1.2, G2, G3, G4*	**Teaching:** -Explain method and give examples of choosing approriate fliplops in term of circuit cost and latency	*A1, A2*

	Timing		optimization. **Learning:** - Asking, answering and discussing. - Reading reference textbook 1: 6.12-6.13 from pages 257 to 262. - Do related exercises in the main reference book. Read the content of the next session.	
Week 5	**Chapter 2: Storage Components** 2.1. Registers 2.2. Shift Registers 2.3. Counters 2.4. BCD Counter 2.5. Asynchoronous Counter	*G1.1, G1.2, G2, G3, G4*	**Teaching:** -Introduce and discuss with students different types of storage components. **Learning:** - Asking, answering and discussing. - Reading reference textbook 1: 7.1-7.5 from pages 268 to 280. - Do related exercises in the main reference book. Read the content of the next session.	*A1, A2*
Week 6	**Chapter 2: Storage Components (cont.)** 2.6. Register File 2.7. Random-Access Memories 2.8. Push-Down Stacks 2.9. First-in-First-out Queue	*G1.1, G1.2, G2, G3, G4*	**Teaching:** -Introduce and discuss with students different types of storage components. **Learning:** - Asking, answering and discussing. - Reading reference textbook 1: 7.6-7.9 from pages 281 to 301. - Do related exercises in the main reference book. Read the content of the next session.	*A1, A2*
Week 7	**Chapter 2: Storage Components (cont.)** 2.10. Simple Datapath 2.11. General Datapath 2.12. Control Unit Design	*G1.1, G1.2, G2, G3, G4*	**Teaching:** -Analyze standard Datapaths and Control units and describe method of building these structures. **Learning:** - Asking, answering and discussing. - Reading reference textbook 1: 7.10-7.12 from pages 268 to 280. - Do related exercises in the main reference book. Read the content of the next session.	*A1, A2*
Week 8	**Midterm Review**	*G1.1, G1.2, G2*	**Teaching:** -Give a short test to review lesson from week 1-7. Correct	

			homeworks pages 263-265, and 316-317 **Learning:** - Asking, answering and discussing. - Do the test and correct homeworks - Review chapter 6 and 7 in textbook for Midterm exam.	
Week 9	**Chapter 3: Register transfer design** 3.1. Design model 3.2. FSMD Definition 3.3. Algorithmic-State Machine Charts 3.4. Synthesis from ASM Charts	*G1.1, G1.2, G2, G3, G4*	**Teaching:** -Lecture, explain, give examples about ASM and models. **Learning:** - Asking, answering and discussing. - Reading reference textbook 1: 8.1-8.4 from pages 320 to 343. - Do related exercises in the main reference book. Read the content of the next session.	*A1, A4*
Week 10	**Chapter 3: Register transfer design** 3.5. Register Sharing 3.6. Functional-Unit Sharing	*G1.1, G1.2, G2, G3, G4*	**Teaching:** Explain and give examples to optimize registers and functional units in Datapath. **Learning:** - Asking, answering and discussing. - Reading reference textbook 1: 8.5-8.6 from pages 343 to 356. - Do related exercises in the main reference book. Read the content of the next session.	*A1, A4*
Week 11	**Chapter 3: Register transfer design** 3.7. Bus Sharing 3.8. Register Merging 3.9. Chaining and Multicycling	*G1.1, G1.2, G2, G3, G4*	**Teaching:** Explain and give examples about bus sharing, register merging, chanining and multicycling in Datapath. **Learning:** - Asking, answering and discussing. - Reading reference textbook 1: 8.7-8.9 from pages 356 to 365. - Do related exercises in the main reference book. Read the content of the next session.	*A1, A4*
Week 12	**Chapter 3: Register transfer design** 3.10. Functional Unit Pipelining 3.11. Datapath pipelining	*G1.1, G1.2, G2, G3, G4*	**Teaching:** Analyze and explain pipeline technique for control unit and datapath. **Learning:**	*A1, A4*

	3.12. Control pipelining 3.13. Scheduling		- Asking, answering and discussing. - Reading reference textbook 1: 8.10-8.13 from pages 365 to 384. - Do related exercises in the main reference book. Read the content of the next session.	
Week 13	**Chapter 4: Processor Design** 4.1. Instruction Sets 4.2. Addressing Modes 4.3. Processor design 4.4. Instruction set design	*G1.1, G1.2, G2, G3, G4*	**Teaching:** Introduce concepts related to processor design. **Learning:** - Asking, answering and discussing. - Reading reference textbook 1: 9.1-9.4 from pages 391 to 405. - Do related exercises in the main reference book. Read the content of the next session.	*A1, A4*
Week 14	**Chapter 4: Processor Design** 4.5. CISC design 4.6. RISC design 4.7. Data forwarding 4.8. Branch prediction	*G1.1, G1.2, G2, G3, G4*	**Teaching:** Introduce instruction set of CISC and RISC processor, explain datapath of these processors, and the technique to handle hazards in pipelining. **Learning:** - Asking, answering and discussing. - Reading reference textbook 1: 9.5-9.9 from pages 391 to 405. - Do related exercises in the main reference book. Read the content of the next session.	*A1, A4*
Week 15	**Endterm Review**	*G1.1, G1.2, G2*	**Teaching:** -Give a short test to review lessons from week 9-14. Correct homeworks in the textbook chapter 8 and 9. **Learning:** - Asking, answering and discussing. - Do the test and correct homeworks - Review chapter 8 and 9 in textbook for Endterm exam.	

b. Lab (Thực hành)

Table 4.

LAB (*5 lab-hours*)	**Contents** *[2]*	**Course learning outcomes**	**Activities** *[4]*	**Assessment element** *[5]*

		[3]		
Lab 1	*Lab 1:* Design a synchronous counter capable of loading the initial value.	*G1, G2*	**Teaching**: Instruct students to perform lab 1, support students with difficult parts in the lab **Learning**: - Prepare at home the design of the synchronous counter. - Perform the lab on Quartus software, verify the design by Quartus simulation and verify on KIT DE2. - Student report lab at class.	*A3*
Lab 2	*Lab 2:* Design Finite State Machine (Moore and Mealy types)	*G1, G2*	**Teaching**: Instruct students to perform lab 2, support students with difficult parts in the lab **Learning**: - Prepare at home steps to design a Moore or Mealy FSM. - Perform the lab on Quartus software, verify the design by Quartus simulation and verify on KIT DE2. - Student report lab at class.	*A3*
Lab 3	*Lab 3:* Design ALU	*G1, G2*	**Teaching**: Instruct students to perform lab 3, support students with difficult parts in the lab **Learning**: - Prepare at home the design of ALU. - Perform the lab on Quartus software, verify the design by Quartus simulation and verify on KIT DE2. - Student report lab at class.	*A3*
Lab 4	*Lab 4:* Design a simple datapath for a specific problem, using ALU designed in lab 3.	*G1, G2*	**Teaching**: Instruct students to perform lab 4, support students with difficult parts in the lab **Learning**: - Prepare at home the theory and steps to design a datapath for a specific problem. - Perform the lab on Quartus software, verify the design by Quartus simulation and verify on KIT DE2. - Student report lab at class.	*A3*
Lab 5	*Lab 5:* Design Control Unit for a specific problem.	*G1, G2*	**Teaching**: Instruct students to perform lab 5, support students with difficult parts in the lab **Learning**: - Prepare at home the design of the	*A3*

			control unit. - Perform the lab on Quartus software, verify the design by Quartus simulation and verify on KIT DE2. - Student report lab at class.	
Lab 6	*Lab 6:* Combine Datapath in Lab 4 and Control unit in Lab 5 to create a simple processor for a specific problem.	*G1, G2*	**Teaching**: Instruct students to perform lab 6, support students with difficult parts in the lab **Learning**: - Prepare at home the design of the processor. - Perform the lab on Quartus software, verify the design by Quartus simulation and verify on KIT DE2. - Student report lab at class.	*A3*

6. COURSE ASSESSMENT (Đánh giá môn học)

Table 5.

Assessment element *[1]*	**Course learning outcomes (Gx)** *[2]*	**Percentage (%)** *[3]*
A1. Others (In-class test, attendance, presentation …)	*G1.1, G1.2, G3, G4*	*10%*
A2. Mid-term exam	*G1.1, G1.2, G2, G4*	*20%*
A3. Lab	*G1.1, G1.2*	*20%*
A4. Final exam	*G1.1, G1.2, G2, G4*	*50%*

a. Rubric Assessment for A1

	(9-10đ)	*(7-8đ)*	*(5-6đ)*	*(3-4đ)*	*(0-2đ)*
Answer questions and do classroom exercises	*Volunteer to answer and do the exercises 4 - 5 times.*	*Volunteer to answer and do the exercises 3 times.*	*Volunteer to answer and do the exercises 2 times.*	*Volunteer to answer and do the exercises 1 time.*	*Volunteer to answer and do the exercises 0 time.*
Check of attendance	*Attend 100% classes.*	*Attend 75% classes.*	*Attend 50% classes.*	*Attend 25% classes.*	*Attend no class.*
Homeworks/ Classroom test	*Understand and do correctly 80 đến 100%*	*Understand and do correctly 60 đến 80%*	*Understand and do correctly 50 đến 60%*	*Understand and do correctly 30 đến 50%*	*Understand and do correctly under 30%*

b. Rubric Assessment for A2

	(9-10đ)	*(7-8đ)*	*(5-6đ)*	*(3-4đ)*	*(0-2đ)*
Design Finite State Machine	*Derive necessary equations for flipflop inputs and the outputs of FSM.*	*Apply algorithm to optimize the number of filpflops used. Know how to encode sates and choose flipflop types.*	*Know the process to synthesize a FSM. Draw state transition diagram.*	*Identify types of FSM model: Moore and Mealy.*	*Not know how to analyze or synthesize a FSM.*
Design Data path, Control path ***Convert algorithm into hardware reality: Datapath & Control Unit***	*Complete the design of the Control Unit.*	*Know how to convert from algorithm to the state machine model for the control unit. Identify the control words of the Control Unit.*	*Know how to build the algorithm for the problem, and decide datapath for the problem*	*Know the operation of basic functional units: registers, shift registers, ALU, counters… to put in the datapath.*	*Not know how to build Datapath and Control Unit.*

c. Rubric assessment for A3

Lab content	*(9-10đ)*	*(7-8đ)*	*(5-6đ)*	*(3-4đ)*	*(0-2đ)*
Design a synchronous counter capable of loading initial value.	*Know how to test the behavior of the counter on KIT DE2*	*Know to use Quartus simulation to verify the design.*	*Know how to build the load circuit for the counter.*	*Know to use quartus to draw the counter circuit.*	*Don't know how to design synchronous counter.*
Design Moore/Mealy state machine	*Know how to test the behavior of Moore-type state machines on KIT DE2*	*Know to use Quartus simulation to verify the design*	*Know how to set up necessary expressions and draw a detailed circuit for the state machine.*	*Know how to create a state transition diagram based on the Moore / Mealy model from the problem description.*	*Don't know how to design a Moore / Mealy type state machin*
Design ALU	*Know how to test the behavior of the ALU on KIT DE2*	*Know to use Quartus simulation/LogiSim to verify the design*	*Design ALU to perform addition, subtraction, overflow.*	*Design ALU with basic functions And, OR, XOR.*	*Don't know how to design ALU.*
Design Datapath	*Know how to test the operation of datapath on KIT DE2*	*Know to use Quartus simulation to verify the design.*	*Know the selection and match the appropriate function blocks to build Datapath to solve the problem.*	*Know how to build algorithms to implement math problems.*	*Don't know how to design Datapath.*
Design Control Unit	*Know how to test operation of Control unit on KIT DE2*	*Know to use Quartus simulation to verify the design*	*Know how to build a state transition diagram and design the state machine for the Control Unit.*	*Know how to set up Control Word for Datapath.*	*Don't know how to design Control Unit..*
Combine Data path and Control unit in a simple	*Know how to test the behavior of the processor on KIT DE2*	*Know to use Quartus simulation to verify the design*	*Optimizing Datapath and Control Unit for the problem.*	*Know how to combine Datapath and Control Unit.*	*Don't know how to pair Datapath and Control Unit.*

processor					

d. Rubric assessment for A4

	(9-10đ)	***(7-8đ)***	***(5-6đ)***	***(3-4đ)***	***(0-2đ)***
Design at RTL level	*Know how to optimize the datapath using register sharing, functional unit sharing*	*Know how to convert FSMD or ASM model into the implementation of a control unit and a datapath.*	*Know how to build FSMD or ASM model for a problem.*	*Understand basic knowledge related FSMD, ASM, and techniques to optimize datapath.*	*Don't understand FSMD, ASM, and techniques to optimize datapath.*
	(9-10đ)	***(7-8đ)***	***(5-6đ)***	***(3-4đ)***	***(0-2đ)***
Processor design	*Know how to apply pipeline for the RISC processor design and handle the hazards.*	*Understand the datapath of RISC and CISC processor, ASMs for CISC and RISC instructions, and know how to build these ASMs.*	*Know how to choose instruction set for a processor.*	*Understand basic knowledge related to instruction set of a processor.*	*Don't understand concepts related to processor design.*

7. COURSE REQUIREMENTS AND EXPECTATIONS (Quy định của môn học)

According to school regulations.

Students must do classroom exercises, prepare answers to questions, finish homeworks, and read the materials required by the instructor before each lesson.

Students are not allowed to be absent for more than 3 lectures during theoretical sessions, and not to be absent for more than 2 labs during the practical sessions. If violating, the students are prohibited to attent the endterm exam.

8. COURSE MATERIALS (Tài liệu học tập, tham khảo)

Textbook

1. Daniel D. Gajski (1997). Principles of digital design. Prentice Hall International Editions.

Reference book

1. Norman Balabanian (2000). *Digital Logic Design Principles 1th Edition*. Nhà xuất bản Wiley Editions.

9. SOFTWARE, TOOLS (Phần mềm, công cụ hỗ trợ thực hành)

1. Software: Altera Quartus Web Edtition.
2. Kit: Altera DE2

HCMC, Jan 15th, 2019

Faculty Head	**Instructor**
(Ký và ghi rõ họ tên)	*(Ký và ghi rõ họ tên)*